DR. SAMUEL GEORGE INSTITUTE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

COURSE STRUCTURE & DETAILED SYLLABUS (SGIT R25)

FOR

M. Tech Two Year Degree Programme

(Applicable for the batches admitted from the A.Y. 2025-26)

ECE – DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING

Dr. SAMUEL GEORGE INSTITUTE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institute with NAAC 'A' Grade)

(Approved by AICTE, New Delhi, Permanently affiliated to JNTUK Kakinada)

(Recognized Under Section 2(f) & 12(B) of UGC, An ISO 9001:2015 Certified Institution)

SGIT B.O – 523320, George Town, Darimadugu (V), MARKAPUR (M), Prakasam (Dist.), A.P.

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SGIT B.O - 523320, George Town, Darimadugu (V), MARKAPUR (M), Prakasam Dist., A.P., India.
e-mail: sgit.principal@gmail.com | Website: www.drsgiet.ac.in | University College Code: 35
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – I Semester

S. No	Course Code	Course Title		Periods / Week			Credits
				L	T	P	
1	**D2513701**	Mathematical Foundation for Communication Engineering		3	1	0	4
2	**D2513702**	Digital System Design		3	1	0	4
3	**D2513703**	Wireless Communications & Networks		3	1	0	4
4	**Program Elective – I**	**D25137A0**	Software Defined Radio	3	0	0	3
		D25137A1	Optical Communication & Networks				
		D25137A2	Radio and Navigational Aids				
5	**Program Elective – II**	**D25137B0**	FPGA and ASIC Design	3	0	0	3
		D25137B1	System Design with RTOS & Embedded LINUX				
		D25137B2	System Design Using Verilog				
6	**D2513790**	Digital System Design Lab		0	1	2	2
7	**D2513791**	Wireless Communications Lab		0	1	2	2
8	**D2513780**	Seminar-I		0	0	2	1
TOTAL				**15**	**5**	**6**	**23**

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COURSE STRUCTURE

M-Tech – II Semester

S. No	Course Code	Course Title		Periods / Week			Credits
				L	T	P	
1	**D2523701**	Information Theory and Coding		3	1	0	4
2	**D2523702**	IoT & its Communication Protocols		3	1	0	4
3	**D2523703**	Embedded System Design		3	1	0	4
4	**Program Elective – III**	**D25237A0**	Design for Testability	3	0	0	3
		D25237A1	MEMS				
		D25237A2	System on Chip Design				
5	**Program Elective – IV**	**D25237B0**	Detection and Estimation Theory	3	0	0	3
		D25237B1	EMI/ EMC				
		D25237B2	ARM Controllers and Embedded C				
6	**D2523790**	Internet of Things Lab		0	1	2	2
7	**D2523791**	Embedded System Design Lab		0	1	2	2
8	**D2523780**	Seminar-II		0	0	2	1
TOTAL				**15**	**5**	**6**	**23**

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2513701	**MATHEMATICAL FOUNDATION FOR COMMUNICATION ENGINEERING**	3	1	0	4	40	60	100

Course Objectives:

1. To introduce foundational concepts of probability, sampling distributions, estimation, and hypothesis testing for statistical data analysis.
2. To develop analytical skills to handle random processes and Markov chains essential in stochastic modelling and simulation.
3. To acquire computational techniques for solving numerical problems involving interpolation, root finding, ODEs, and eigenvalue problems.
4. To explore mathematical optimization through multivariable calculus, constrained optimization techniques, and numerical methods.
5. To introduce wavelet transform concepts and their application to multi-resolution analysis in data and signal processing.

Unit–I: Probability and Statistics:

Sampling distributions, Estimation of parameters (point estimation – unbiasedness & minimum variance, basics of interval estimation – confidence interval for mean), Testing of hypotheses (one and two sample tests for mean), Linear regression, Introduction to non-linear regression.

Unit-II: Stochastic process:

Random processes, Random walk, Markov process with special emphasis on Markov chain

Unit–III: Numerical Analysis:

Introduction to Interpolation formulae [Bessel's & Sterling's], Roots of transcendental equations [Bisection, Regula-Falsi & Newton-Raphson] Solutions of simultaneous non-linear equations [Newton's method], Numerical solution of Ordinary Differential equation

[Modified Euler's method, fourth order Runga-Kutta method], Matrix Eigen value and Eigen vector problems.

Unit-IV: Optimization Technique:

Calculus of several variables, Implicit function theorem, Nature of singular points, Necessary and sufficient conditions for optimization, Constrained Optimization, Lagrange multipliers, Gradient method – steepest descent method.

Unit-V: Wavelet Transform:

Resolution problems, Multi-resolution analysis, Continuous & discrete wavelet transform

TEXT BOOKS:

1. 1.A. Papoulis and S. Unnikrishnan Pillai, ``Probability, Random Variables and Stochastic Processes," Fourth Edition, McGraw Hill. (Indian Edition is available).
2. Gibert Strang," Linear Algebra and its applications", Thomson Learning Inc, 4th Edition.

REFERENCE BOOKS:

1. H.Stark and J. Woods, 'Probability and Random Processes with Applications to Signal Processing," Third Edition, Pearson Education. (Indian Edition is available).
2. Steven M. Kay, " Intuitive Probability and Random Process using MATLAB", Springer Publications.
3. Todd K Moon, Wynn C. Stirling" Mathematical Methods and Algorithms for Signal Processing, Prentice Hall.

Course Outcomes: By the end of this course, students will be able to:

1. Apply statistical methods including point estimation, confidence intervals, and hypothesis testing to real-world data scenarios.
2. Model and analyze stochastic systems using random processes, random walks, and Markov chains.
3. Solve engineering and scientific problems using numerical techniques such as Newton-Raphson, interpolation methods, and Runge-Kutta for differential equations.
4. Perform optimization tasks with or without constraints using gradient-based techniques and understand the role of Lagrange multipliers.
5. Use wavelet transforms to analyze signals and data with applications in compression and resolution enhancement.

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2513702	**DIGITAL SYSTEM DESIGN**	3	1	0	4	40	60	100

Course Objectives:

1. To design digital circuits, behaviour and RTL modelling of digital circuits using verilog HDL, verifying these Models and synthesizing RTL models to standard cell libraries and FPGAS.
2. To gain practical experience by designing, modelling, implementing and verifying several digital
3. To provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using software tools

UNIT - I:

Introduction to VerilLog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II:

Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

UNIT -III:

Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators,Design at dataflow level, Parameter and constant usage in dataflow.

UNIT - IV:

Behavioural Modelling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioural Level

UNIT -V:

Verilog Procedural and Control Constructs: Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

TEXT BOOKS:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. ZainalabdienNavabi, Verliog Digital System Design, TMH, 2nd Edition.

REFERENCE BOOKS:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL -Michel D. Ciletti, PHI,2009.

COURSE OUTCOMES: By the end of this course, students will be able to:

1. Use Verilog hardware description languages(HDL)
2. Design digital circuits
3. Explore behavioral models of digital circuits
4. Analyse Register Transfer Level (RTL) models of Digital Circuits
5. Verify Behavioral and RTL models

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2513703	**WIRELESS COMMUNICATIONS & NETWORK**	3	1	0	4	40	60	100

COURSE OBJECTIVES:

1. To introduce the cellular system design concepts including frequency reuse, interference management, and handoff strategies.
2. To understand large-scale radio wave propagation models and their impact on wireless system performance.
3. To study small-scale fading, multipath propagation effects, and statistical models for channel behavior.
4. To explore equalization and diversity techniques for improving signal quality in wireless environments.
5. To provide an overview of wireless networks and standards such as IEEE 802.11, IEEE 802.16, and wireless PANs.

UNIT-I:

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring, Channel Assignment Strategies, Handoff Strategies-Prioritizing Handoffs, Practical Handoff Considerations, Trunking and Grade of Service

UNIT-II:

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, Basic Propagation Mechanisms,

Reflection: Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection(Two-Ray) Model.

Diffraction: Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, HataModel, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance pathloss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT-III:

Mobile Radio Propagation: Small –Scale Fading and Multipath Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel-Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to DopplerSpread Fastfading,slowfading,StatisticalModelsformultipathFadingChannels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and GansFadingModel, Levelcrossingandfadingstatistics, Two-rayRayleighFadingModel.

UNIT-IV:

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training a Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non-linear Equalization-Decision Feedback Equalization(DFE), Maximum Likelihood Sequence Estimation(MLSE)Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT-V:

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE802.11, IEEE802.11Medium Access Control, Comparison of IEEE802.11a,b,g and n standards, IEEE802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

1. Wireless Communications, Principles, Practice– heodore, S.Rappaport, 2ndEd.,2002, PHI.
2. WirelessCommunications-AndreaGoldsmith,2005CambridgeUniversityPress,1st Edition.
3. Mobile Cellular Communication–Gottapu Sasibhushana Rao, Pearson Education India, First Edition, 2012.

REFERENCEBOOKS:

1. Principles of Wireless Networks – KavehPahLaven and P.KrishnaMurthy, 2002, PE
2. Wireless Digital Communications–KamiloFeher,1st edition 1995,Prentice-Hall PTR.
3. Wireless Communications and Networks by William Stallings — 2nd Edition (2005), Pearson Prentice Hall.

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Explain the fundamentals of cellular system design including frequency reuse and interference management.
2. Analyze the behaviour of radio wave propagation using large-scale path loss models.
3. Evaluate the impact of small-scale fading and multipath propagation using appropriate statistical models.
4. Apply equalization and diversity techniques to mitigate fading and improve signal reception.
5. Compare various wireless network standards and demonstrate their applicability in real-world scenarios.

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25137A0	**SOFTWARE DEFINED RADIO (Programme Elective I)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. Introduce the evolution of radio communication systems and the fundamental concepts, architectures, and design principles of Software Defined Radio (SDR).
2. Understand the implementation challenges in RF front-end systems, including dynamic range, receiver topologies, and performance-affecting factors.
3. Explore digital signal generation techniques, particularly direct digital synthesis (DDS), and analyse related spurious signal behaviours.
4. Introduce multidate signal processing methods such as sample rate conversion, polyphase filters, and timing recovery in digital receivers.
5. Study analogy-to-digital and digital-to-analogy conversion techniques and methods for improving data converter performance in SDR systems.

UNIT I:

Introduction to Software radio concepts: Introduction, need, characteristics, benefits and design principles of Software Radios. Traditional radio implemented in hardware (first generations of 2G cell phones), Software controlled radio (SCR), Software defined radio (SDR), Ideal software radio (ISR), Ultimate software radio (USR)

UNIT II:

Radio frequency implementation issues: The purpose of RF Front-End, Dynamic range, RF Receiver Front-End Topologies, Enhanced Flexibility of the RF Chain with Software Radios, Importance of Components to Overall performance, Transmitter Architecture and their issues, Noise and Distortion in RF Chain.

UNIT III:

Digital generation of signals: Introduction, Comparison of Direct Digital Synthesis with Analog Signal Synthesis, Approaches to Direct Digital Synthesis, Analysis of Spurious Signals, Spurious components due to Periodic Jitter.

UNIT – IV:

Multirate Signal Processing: Introduction, Sample Rate Conversion Principles, Polyphase Filters, Digital Filter Banks, Timing Recovery in Digital receivers Using Multirate Digital Filters.

UNIT – V:

A/D & D/A Conversion: Introduction, Parameters of Ideal Data Converters, Parameters of Practical data Converters, Techniques to improve Data Converter performance, JTRS.

TEXTBOOKS:

1. Jeffery H. Reed, "Software Radio, (A modern approach to radio engineering)", PHI PTR, 2002
2. John J. Rouphael, "RF and Digital Signal Processing for Software Defined Radio" Elsevier, Newness Publications.

REFERENCE BOOKS:

1. C. Richard Johnson, Jr., and William A. Sethares, Telecommunication Breakdown, Prentice Hall, ISBN 0-13-143047-5, 2004
2. Software Defined Radio: Theory and Practice by John M. Reyland (Artech House, 2023)

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Understand the fundamentals of Software Radios, their evolution from traditional radios, and the various levels including SCR, SDR, ISR, and USR.
2. Analyse RF front-end architectures, dynamic range requirements, and the role of RF components in system performance for Software Radio implementation.
3. Explain and compare different signal generation techniques including direct digital synthesis, and analyse sources of spurious components and jitter effects.
4. Applymulti-rate signal processing techniques such as sample rate conversion, polyphase
5. Evaluate the performance of A/D and D/A converters in practical systems, and describe methods to improve conversion performance, including relevance to JTRS

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M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25137A1	**OPTICAL COMMUNICATION & NETWORKS (Programme Elective I)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. Introduce the fundamentals of optical fiber communication, including transmission link components, light propagation, and fiber structures.
2. Understand the principles and performance of optical sources and detectors used in optical communication systems.
3. Explain the structure and function of optical communication systems, including digital systems and modern high-speed links.
4. Familiarize students with components and technologies used in fiber optic networks and their architectures.
5. Explore coherent communication systems, detection techniques, and the role of demodulation and noise management in optical receivers.

UNIT-I: Overview of optical fiber communications: Elements of an optical fiber transmission link. Optical Fibers: structures, wave guiding, Nature of light, Basic optical laws and definitions, optical fiber modes and configurations (Fiber types, Rays and modes, step index and graded index fibers) mode theory of circular wave guides. (Qualitative Treatment) Fabrication, cabling and installation: Fabrication, fiber optic cables, Installation-placing the cable.

UNIT-II: Optical sources: LEDs, structures, quantum efficiency, modulation capability, Laser diodes: Laserdiodes and threshold conditions, external quantum efficiency resonant frequencies, Optical Detectors: Physical principles of photodiodes (pin Photodiode, avalanche, photodiode) comparison of photodetectors, noise in detectors.

UNIT-III: Optical Communication Systems: Block diagrams of optical communication systems, direct intensity modulation, digital communication systems, Laser semiconductor

transmitter, Generations of optical fiber link, description of 8Mb/s optical fiber communication link, description of 2.5Gb/s optical fiber communication link.

UNIT-IV: Components of fiber Optic Networks: Overview of fiber optic networks, Transreceiver, semiconductors optical amplifiers, couplers/splicer's, wavelength division multiplexers and demultiplexers, filters, isolators and optical switches. Fiber Optic Networks: Basic networks, SONET/SDIT, Broadcast and select WDM Networks, wavelength routed networks, optical CDMAN on-linear effects on network performance.

UNIT-V: Coherent Systems: Coherent receiver, Homodyne and hetero dyne detection, noise in coherent receiver, polarization control, Homodyne receiver, Reusability and laser line width, heterodyne receiver, synchronous, Asynchronous and self-synchronous demodulation, phase diversity receivers.

TEXTBOOKS:

1. Optical fiber communications–GerdKeiser,3rdEd.MGH.
2. Fiber Optic Communication Technology–Djafar K.Mynbaev and LowellL. Scheiner,
3. Opto electronic devices and systems –S.C.Gupta ,PHI, 2005.

REFERENCEBOOKS:

1. Fiber Optics Communications –HaroldKolimbiris (Pearson Education Asia)
2. Optical Fiber Communications and its applications–S.C.Gupta(PHI)2004.

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Explain the fundamental principles of optical fiber communication including waveguiding, fiber types, and mode theory of circular waveguides.
2. Compare and analyze various optical sources (LEDs, laser diodes) and detectors (PIN, APD) in terms of efficiency, modulation capability, and noise performance.
3. Design and interpret the block diagrams of optical communication systems and explain the working of digital systems including 8 Mb/s and 2.5 Gb/s optical links.
4. Evaluate different fiber optic network components such as transceivers, amplifiers, WDM Systems.
5. Demonstrate understanding of coherent optical systems including homodyne/heterodyne detection, polarization effects, and noise handling in coherent receivers.

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25137A2	**RADIO AND NAVIGATIONAL AIDS (Programme Elective I)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. Understand the principles and configurations of radio positioning systems and factors affecting positioning accuracy.
2. Explore terrestrial radio navigation systems including LORAN, ILS, and indoor/urban positioning technologies.
3. Introduce fundamental navigation concepts such as position fixing, dead reckoning, and integrated navigation systems.
4. Study advanced satellite navigation techniques including Differential GNSS and carrier phase positioning.
5. Examine inertial navigation systems and their equations, alignment methods, and error propagation models.

UNIT I: Principles of Radio Positioning: Radio Positioning Configurations and Methods, Positioning Signals, User Equipment, Propagation, Error Sources, and Positioning Accuracy. Terrestrial Radio Navigation: Point-Source Systems, Loran, Instrument Landing System, Urban and Indoor Positioning, Relative Navigation, Tracking, Sonar Transponders.

UNIT II: Introduction To Navigation: What Is Navigation, Position Fixing, Dead Reckoning, Inertial Navigation, Radio and Satellite Navigation, Terrestrial Radio Navigation, Satellite Navigation, Feature Matching, The Complete Navigation System.

UNIT III: Advanced Satellite Navigation: Differential GNSS, Carrier-Phase Positioning and Attitude, Poor Signal-to-Noise Environments, Multipath Mitigation, Signal Monitoring, Semi Codeless Tracking.

UNIT IV: Inertial Navigation: Inertial-Frame Navigation Equations, Earth-Frame Navigation Equations, Local-Navigation-Frame Navigation Equations, Navigation Equations Precision, Initialization and Alignment, INS Error Propagation, Platform INS, Horizontal Plane Inertial Navigation.

UNIT V: Satellite Navigation & GNSS Systems: Fundamentals: GPS, GLONASS, Galileo, Beidou, IRNSS, signal structure, measurement errors (ionospheric/tropospheric/multipath), Dilution of Precision (GDOP, PDOP), ephemeris, clock/correction errors, Differential GNSS, WAAS, integrity monitoring, carrier-phase techniques.

TEXTBOOKS:

1. G S RAO, Global Navigation Satellite Systems, McGraw-Hill Publications, New Delhi, 2010.
2. Principles of GNSS, Inertial, and Multisensor Integrated Navigation Systems, Paul D. Groves Artech House, 2008 and 2013 Second Edition.
3. B. Hofmann Wollenhof, H. Lichtenegger, and J. Collins, "GPS Theory and Practice", Springer Wien, New York, 2000.

REFERENCE BOOKS:

1. Pratap Misra and Per Enge, "Global Positioning System Signals, Measurements, and Performance," Ganga-Jamuna Press, Massachusetts, 2001.
2. Ahmed El-Rabbany, "Introduction to GPS," Artech House, Boston, 2002.
3. Bradford W. Parkinson and James J. Spilker, "Global Positioning System: Theory and Applications," Volume II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.

COURSEOUTCOMES: After completion of the course, students will be able to:

1. Explain the principles, configurations, and error sources of terrestrial and radio positioning systems.

2. Apply various navigation methods to determine position and trajectory.

3. Analyse advanced satellite navigation techniques for accuracy enhancement.

4. Evaluate inertial navigation equations, alignment methods, and error propagation.

5. Integrate GNSS systems with error correction techniques for reliable navigation solutions.

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COURSE STRUCTURE

M-Tech – I Semester

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		L	T	P	C			
D25137B0	**FPGA AND ASIC DESIGN (Programme Elective II)**	3	0	0	3	40	60	100

COURSE OUTCOMES:

1. To introduce the evolution, design flow, and applications of FPGAs and PLDs.
2. To study various FPGA/CPLD programming technologies and commercially available devices.
3. To understand the internal architecture and building blocks of FPGAs/CPLDs and their impact on performance.
4. To explore routing architectures and strategies used in different FPGA types.
5. To analyse architectural elements and apply FPGA technology in real-world case studies.

UNIT-I:

Introduction to FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.Design Examples Using PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter

UNIT-II:

FPGAs/CPLDs: Programming Technologies, commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.

UNIT-III:

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT-IV:

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in

symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures

UNIT-V:

FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA Case Study – Applications using Kintex-7, Virtex-7, Artix-7.

TEXT BOOKS:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
2. VLSI Design: A Practical Guide for FPGA and ASIC Implementations by Vikram A. Chandrasetty (SpringerBriefs, 2011).

REFERENCE BOOKS:

1. Data sheets of Artix-7, Kintex-7, Virtex-7.
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Explain the evolution, design flow, and practical applications of FPGAs and PLDs.
2. Compare different FPGA/CPLD devices and their programming technologies.
3. Analyse the architecture of logic blocks, routing structures, and I/O blocks in FPGAs.
4. Apply routing techniques to various FPGA architectures for optimized performance.
5. Demonstrate FPGA design implementation using case studies on Kintex-7, Virtex-7, and Artix-7.

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25137B1	**SYSTEM DESIGN WITH RTOS & EMBEDDED LINUX (Programme Elective II)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. To introduce the key concepts of Real-Time Operating Systems and task management fundamentals.
2. To explore synchronization and communication mechanisms used in real-time systems.
3. To understand the role of exceptions interrupts, and timer services in RTOS environments.
4. To provide hands-on experience with Linux kernels and shell scripting for embedded applications.
5. To analyse embedded Linux architecture and understand the process of application porting and driver integration.

UNIT I: Introduction to RTOS and Task Management

Introduction to Real-Time Operating Systems (RTOS): Key characteristics, scheduler, kernel objects and services, system calls, static and dynamic libraries, cross tool chains, Task management: Defining tasks, task states, scheduling, task operations, synchronization, communication, concurrency.

UNIT II: Synchronization, Communication, and I/O Systems

Semaphores: Operations use cases, Message Queues: Types, operations, use cases (including pipes, event registers, signals, condition variables), I/O Subsystems: I/O concepts, subsystems, Synchronization and Communication: Resource synchronization methods, critical section, design patterns, priority inversion, common design problems (deadlocks, priority inversion).

UNIT III: Exceptions, Interrupts, and Timer Services

Exceptions and Interrupts: Definitions, applications, spurious interrupts, Timer Services: Real-time clocks, system clocks, programmable interval timers, timer interrupt service routines.

UNIT IV: Linux Kernel and Shell Scripting

Introduction to Linux Kernels: Linux basics, GNU utilities, distributions, access methods (CLI, graphical terminal emulators), Bash Shell Commands: Navigation, file handling, system monitoring, environment variables, user-defined variables, Shell Scripting: Script creation, control structures (if-else, loops, case commands), output redirection, practical examples, handling signals, background scripts, basic script functions, alternative shells (dash, zsh)

UNIT V: Embedded Linux Architecture and Application Porting

Embedded Linux Architecture: Kernel architecture, memory manager, scheduler, file system, I/O and networking subsystems, IPC, user space, startup sequence, Board Support Package: Embedded storage (MTD), embedded file system, embedded device drivers (communication between user space and kernel, character/block drivers, interrupt handling, kernel modules), Porting Applications: Real-time Linux, hard real-time programming, building and debugging (bootloaders, kernel, root file system, device tree).

TEXTBOOKS:

1. Qing Li, Caroline Yao (2020), "Real-Time Concepts for Embedded Systems", CMP Books.
2. Chris Simmonds, "Mastering Embedded Linux Programming" - Second Edition, PACKT Publications Limited.

REFERENCE BOOKS:

1. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates.
2. Mastering Embedded Linux Programming (3rd Edition) by Frank Vasquez & Chris Simmonds.

COURSE OUTCOMES: After completing the course, students will be able to:

1. DescribeRTOS features, kernel components, and manage task scheduling and synchronization.
2. Implementinter-task communication using semaphores, message queues, and handle I/O operations effectively.
3. Analyze the behaviour of exceptions, interrupts, and use timer services in real-time systems.
4. Use Linux shell commands and scripts to perform system-level operations and automation tasks.
5. Demonstrate understanding of embedded Linux internals and port applications with BSP and device drivers.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25137B2	**SYSTEM DESIGN USING VERILOG (Programme Elective II)**	3	0	0	3	40	60	100

COURSE OBJECTIVES: This course teaches:

1. Designing digital circuits, behaviour and RTL modelling of digital circuits using Verilog HDL, verifying these Models and synthesizing RTL models to standard cell libraries and FPGAS.
2. Students gain practical experience by designing, modelling, implementing and verifying several digital
3. This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools.

UNIT - I:

Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II:

Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

UNIT -III:

Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators, Design at dataflow level,

Parameter and constant usage in dataflow.

UNIT - IV:

Behavioural Modelling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioural Level

UNIT -V:

Verilog Procedural and Control Constructs: Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

TEXTBOOKS:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. ZainalabdienNavabi, Verilog Digital System Design, TMH, 2nd Edition.

REFERENCE BOOKS:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown,ZvonkocVranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL -Michel D. Ciletti, PHI,2009.

COURSE OUTCOMES: By the end of this course, students should be able to:

1. Describe Verilog hardware description, languages(HDL).
2. Design digital circuits.
3. Write Behavioural models of digital circuits.
4. Write Register Transfer Level (RTL) models of Digital Circuits
5. Verify Behavioural and RTL models.

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SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2513790	**DIGITAL SYSTEM DESIGN LAB**	0	1	2	2	40	60	100

COURSE OBJECTIVES:

1. To introduce algorithms for efficient combinational and sequential logic design such as CAMP-I, CAMP-II, and Kohavi.
2. To familiarize students with programmable logic array (PLA) design, minimization, and folding techniques.
3. To develop skills in the design and implementation of ROM and control logic units.
4. To enable practical experience in digital system implementation using FPGA platforms.
5. To understand and experiment with error detection/correction and finite state machine design concepts.

Systems Design experiments:

- The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
- Consider the suitable switching function and data to implement the required logic if required.

A student has to do at least 10 Experiments

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm)

5. PLA folding algorithm (COMPACT algorithm)
6. ROM design.
7. Control unit and data processor logic design
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Apply CAMP-I and CAMP-II algorithms to determine essential, secondary, and spurious prime implicants.
2. Implement PLA minimization and folding using IISc and COMPACT algorithms respectively.
3. Designand realize ROM-based systems and control/data path logic circuits.
4. Developdigital systems using FPGA tools and platforms for real-time applications.
5. Perform logic minimization using Kohavi's algorithm and analyze error-correcting codes through Hamming experiments.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2513791	**WIRELESS COMMUNICATIONS LAB**	0	1	2	2	40	60	100

COURSE OBJECTIVES:

1. To understand and analyse digital communication techniques including error detection and correction.
2. To provide hands-on experience in spread spectrum systems, convolutional coding, and decoding.
3. To apply signal processing techniques using transforms, filtering, and DSP hardware platforms.
4. To explore image processing operations and study their effects on digital images.
5. To study and experiment with optical fiber communication, mobile phone trainers, CDMA, and ISDN systems.

PART A: List of Experiments :(Minimum of Ten Experiments must be performed)

1. Measurement of Bit Error Rate using Binary Data
2. Verification of minimum distance in Hamming code
3. Determination of output of Convolution Encoder for a given sequence
4. Determination of output of Convolution Decoder for a given sequence
5. Efficiency of DS Spread- Spectrum Technique
6. Simulation of Frequency Hopping (FH) system
7. Effect of Sampling and Quantization of Digital Image
8. Verification of Various Transforms (FT / DCT/ Walsh / Hadamard) on a given Image (Finding Transform and Inverse Transform)
9. Point, Line and Edge detection techniques using derivative operators.
10. Implementation of FIR filter using DSP Trainer Kit (C-Code/ Assembly code)
11. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code)

12. Determination of Losses in Optical Fiber
13. Observing the Waveforms at various test points of a mobile phone using Mobile Phone Trainer
14. Study of Direct Sequence Spread Spectrum Modulation & Demodulation using CDMA- DSSBER Trainer
15. Study of ISDN Training System with Protocol Analyzer
16. Characteristics of LASER Diode.

PART B: Equipment required for Laboratory Software:

1. MATLAB along with Simulink Licensed simulation software tool with communication and Signal processing Toolbox.
2. Computer Systems with required specifications

Hardware:

1. Hardware kits for verification of BER
2. Hardware kits of Convolution encoders, Hamming encoders.
3. Frequency spectrum
4. Mobile Phone Trainer
5. DSP Trainer Kit
6. CDMA-DSS-BER Trainer
7. ISDN Training System with Protocol Analyzer
8. Optical fiber Transmitter and receiver kit along with different lengths of cables

COURSE OUTCOMES: After successful completion of the course, students will be able to:

1. Measure bit error rates and verifyerror correction capabilities using Hamming codes.
2. Simulate and analyseconvolutional encoder/decoder systems and spread spectrum techniques.
3. Implement and evaluate digital signal processing algorithms (FIR/IIR filters) on DSP trainer kits.
4. Apply transforms (FT, DCT, Walsh, Hadamard) and perform edge/line detection in digital images.
5. Experiment with optical fiber characteristics, mobile phone trainer systems, and CDMA/ISDN technologies.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2513780	**SEMINAR-I**	0	0	2	1	100	-	100

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SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)
COURSE STRUCTURE

M-Tech –II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2523701	**INFORMATION THEORY AND CODING**	3	1	0	4	40	60	100

COURSE OBJECTIVES:

1. Introduce core concepts of information theory including entropy and mutual information.
2. Teach lossless source coding algorithms like Huffman, Arithmetic, and LZW.
3. Explain channel capacity and its evaluation for various communication channels.
4. Explore the fundamentals of video and speech coding techniques.
5. Provide knowledge of error control coding for reliable data transmission.

UNIT-I: Introduction

Information Source, Symbols, and Entropy, Mutual information, information Measures for Continuous Random Variable, Joint and Conditional Entropy, Relative Entropy, Applications Based on information Theoretic Approach.

UNIT-II: Source coding

Source Coding Theorem, Kraft inequality, Shannon-Fano Codes, Huffman Codes, Run Length Code, Arithmetic Codes, Lempel-Ziv-Welch Algorithm, Universal Source Codes, Prefix Codes, Variable Length Codes, Uniquely Decodable Codes, instantaneous Codes, Shannon's Theorem, Shannon Fano Encoding Algorithm, Shannon's Noiseless Coding Theorem, Shannon's Noisy Coding Theorem.

UNIT-III: Communication channel

Channel and its Capacity, Continuous and Gaussian Channels, Discrete Memory-Less Channels, Symmetric Channel, Binary Erasure Channel, Estimation of Channel Capacity, Noiseless

Channel, Channel Efficiency, Shannon's Theorem on Channel Capacity, MIMOs Channels, Channel Capacity with Feedback.

UNIT-IV: Video and speech coding

Video Coding Basics, Quantization, Symbol Encoding, Intraframe Coding, Predictive Coding, Transform Coding, Sub band Coding, Vector Quantization, Interframe Coding, Motion Compensated Coding, Image Compression, Jpeg, LZ78 Compression, Dictionary Based Compression, Statistical Modeling, Speech Coding, Psycho-Acousting Modeling, Time Frequency Mapping Quantization, Variable Length Coding, Multichannel Correlation and Irrelevancy, Long Term Correlation, Pre-Echo Control, Bit Allocation.

UNIT-V: Error control coding

Overview of Field, Group, Galois Field, Types of Codes, Hamming Weight, Minimum Distance Based Codes, Error Detection and Error Correction Theorems, Maximum Likelihood Decoder, Map Decoder, Linear Block Codes and Their Properties, Equivalent Codes, Generator Matrix and Parity Check Matrix, Systematic Codes, Cyclic Codes, Convolution Codes and Viterbi Decoding Algorithm, Iterative Decoding, Turbo Codes and Low Density-Parity-Check Codes, Asymptotic Equipartition Property, Bch Codes, Generator Polynomials, Decoding of Bch Codes, Reed Solomon Codes, Trellis Codes, Space Time Coding.

TEXTBOOKS:

1. T.M. Cover and J.A. Thomas, Elements of Information Theory, John Wiley & Sons
2. Todd K. Moon, Error Correction coding, John Wiley, 2005.

REFERENCE BOOKS:

1. Shu lin/ Daniel J.Costello Jr., Error Control Coding, Prentice Hall series in computer applications in electrical engineering series (2/e) 2005.
2. Ranjan Bose, Information Theory, coding and cryptography (2/e), McGraw Hill

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SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2523702	**IOT & ITS COMMUNICATION PROTOCOLS**	3	1	0	4	40	60	100

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Understand and compute entropy, mutual information, and related measures.
2. Apply and analyse source coding algorithms for efficient data compression.
3. Evaluate channel capacity and efficiency in communication systems.
4. Implement and compare video/speech coding and multimedia compression techniques.
5. Design and analyse error control codes for error detection and correction

COURSE OBJECTIVES:

1. Introduce the core architecture and technologies of IoT, including devices, gateways, networking, data management, and services.
2. Familiarize students with IoT reference architectures, views, and the design constraints encountered in real-world implementations.
3. Understand data link and network layer protocols that support communication in IoT systems, including both traditional and IoT-specific protocols.
4. Explore transport and session layer protocols essential for reliable and efficient data transfer in IoT communication models.
5. Explain service layer and security protocols used in IoT systems, emphasizing interoperability and secure communication.

UNIT-I: Introduction: IoT architecture outline, standards - IoT Technology Fundamentals- Devices and gateways, Local and wide areanetworking, Data management, Business processes in IoT, Everything as a Service (XaaS), M2M and IoT Analytics

UNIT-II: IoT Reference Architecture: Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints

UNIT-III: IoT Data Link Layer & Network Layer Protocols: PHY/MAC Layer (3GPP MTC, IEEE 802.11, IEEE 802.15), WirelessHART, Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH7 - Network Layer-IPv4,IPv6, 6LoWPAN, 6TiSCH,ND, DHCP, ICMP, RPL, CORPL, CARP

UNIT-IV: IoT Transport & Session Layer Protocols: Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, CoAP, XMPP, AMQP, MQTT

UNIT-V: IoT Service Layer Protocols & Security Protocols: Service Layer -oneM2M, ETSI M2M, OMA, BBF – Security in IoT Protocols – MAC802.15.4 , 6LoWPAN, RPL, Application Layer

TEXTBOOKS:

1. Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The EvolvingWorld of M2M Communications", ISBN: 978-1-118-47347-4, Willy Publications ,2016
2. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand,StamatisKarnouskos, David Boyle, "From Machine-to-Machine to the Internet ofThings: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2015.

REFERENCE BOOKS:

1. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things",ISBN 978- 3-64219156-5 e-ISBN 978-3-642-19157-2, Springer, 2016
2. N. Ida, Sensors, Actuators and Their Interfaces, Scitech Publishers, 2014.

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SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2523703	**EMBEDDED SYSTEM DESIGN**	3	1	0	4	40	60	100

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Understand the fundamental components and architecture of IoT systems
2. Interpret and apply various IoT reference architectural views
3. Analyze data link and network layer protocols used in IoT communication
4. Evaluate transport and session layer protocols for their suitability in IoT applications
5. Assess IoT service layer and security protocols to ensure interoperability and secure Communication.

COURSE OBJECTIVES:

1. To introduce the fundamentals, classification, and characteristics of embedded systems.
2. To explore the core components of embedded systems including processors, memory, and interfaces. 3. To understand embedded firmware components and design approaches.
3. To study ARM processor architecture, instruction sets, and programming model.
4. To provide practical exposure to Raspberry Pi programming, communication protocols, and sensor interfacing.

UNIT-I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT-II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT-III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

ARM: ARM design philosophy, data flow model and core architecture, registers, program status register, instruction pipeline, interrupts and vector table, operating modes and ARM processor families. Instruction Sets: Data processing instructions, addressing modes, branch, load, store instructions, PSR instructions, and conditional instructions.

UNIT -V

Raspberry Pi: Raspberry Pi board and its processor, Programming the Raspberry Pi using Python, Communication facilities on Raspberry Pi (I2C, SPI, UART), Interfacing of sensors and actuators.

TEXTBOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.
2. A. N. Sloss, D. Symes, and C. Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Elsevier, 2008.
3. S. Monk, "Programming the Raspberry Pi" McGraw-Hill Education, 2013

REFERENCE BOOKS:

1. Steave Furber, "ARM system-on-chip architecture", Addison Wesley, 2000.
2. Embedded Systems: Architecture, Programming and Design is the Second Edition, published in 2008, by Tata McGraw-Hill,- Raj Kamal.
3. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley,1st Edition (2001)

COURSE OUTCOMES: After successful completion of the course, students will be able to:

1. Describe the structure, classification, and purpose of embedded systems and their quality attributes.
2. Analyseembedded system components such as processors, memory types, sensors, actuators, and interfaces.
3. Explain embedded firmware building blocks and apply suitable design approaches.
4. Demonstrate knowledge of ARM architecture and instruction sets relevant to embedded programming.
5. Develop simple embedded applications using Raspberry Pi and interface sensors and communication peripherals.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)
COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25237A0	**DESIGN FOR TESTABILITY (Programme Elective III)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. To introduce the fundamental concepts, types, and philosophies of VLSI testing.
2. To understand fault models and apply logic/fault simulation techniques for test evaluation.
3. To study testability measures and design-for-test (DFT) techniques including scan design.
4. To explore Built-In Self-Test (BIST) strategies and their application in digital systems.
5. To learn the boundary scan architecture and standards used in board-level testing.

UNIT-I: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III: Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern

Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V: Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXTBOOKS:

1. M.L. Bushnell, V. D. Agrawal, "Essential of Electronic Testing for Digital, Memory and MixedSignal VLSI Circuits", Kluwer Academic Publishers.
2. Digital Systems Testing and Testable Design,Author: MironAbramovici, Melvin A. Breuer, Arthur D. Friedman,Publisher: IEEE Press

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design", Jaico Publishing House.
2. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press.

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Explain the role of testing in VLSI systems and differentiate between fault models and testing types.
2. Apply simulation algorithms for design verification and fault analysis in digital circuits.
3. Evaluate testability using measures like SCOAP and design scan-based test structures.
4. Design and implement BIST strategies for logic and memory testing.
5. Demonstrate understanding of boundary scan standards and describe systems using BSDL.

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COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25237A1	**MEMS (Programme Elective III)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. To introduce the fundamentals, materials, and applications of MEMS and smart systems.
2. To explore various types of micro-sensors, actuators, and smart material-based systems.
3. To study micro-fabrication techniques including deposition, lithography, and micromachining. 4. To understand the mechanical modelling of microstructures such as beams, bars, and multilayer elements.
4. To apply numerical analysis techniques like Finite Element Method (FEM) for modelling MEMS structures.

UNIT-I

Introduction to MEMS: Microsystems versus MEMS, Micro fabrication, Smart Materials, Structures and Systems, Integrated Microsystems, Applications of Smart Materials and Microsystems

UNIT-II

Micro Sensors, Actuators, Systems And Smart Materials: Silicon Capacitive Accelerometer, Piezo-resistive Pressure Sensor, Conductometric Gas Sensor, An Electrostatic Comb-Drive, A Magnetic Micro relay, Portable Blood Analyzer, Piezoelectric Inkjet Print Head, Micro-mirror Array for Video ProjectionSmart Materials and Systems

UNIT-III

Micro Fabrication Technique: Silicon as a Material for Micromachining, Thin-Film Deposition,

Lithography, Etching, Silicon Micromachining Specialized Materials for Microsystems, Advanced Processes for Micro fabrication

UNIT-IV

Modeling of Solids In Microsystems: The Simplest Deformable Element: A Bar, Transversely Deformable Element: A beam, Energy Methods for Elastic Bodies, Heterogeneous Layered Beams, Bimorph Effect, Residual Stresses and Stress Gradients, Poisson Effect and the Anticlastic Curvature of Beams, Torsion of Beams and Shear Stresses, Dealing with Large Displacements, In-Plane Stresses

UNIT-V

Finite Element Method: Need for Numerical Methods for Solution of Equations - Variational Principles, Finite Element Method, Finite Element Model for Structures with Piezoelectric Sensors and Actuators, Analysis of a Piezoelectric Bimorph Cantilever Beam

TEXTBOOKS:

1. Fundamentals of Micro fabrication — Marc J. Madou (CRC Press, 1997/2002).
2. An Introduction to Microelectromechanical Systems Engineering — N. Maluf (Artech House,1999).

REFERENCE BOOKS:

1. Micro and Smart Systemsby G.K. Ananthasuresh, K.J. Vinoy,S.Gopalakrishnan,K.N.Bhat, V.K.Aatre: Wiley, India (2016).
2. Smart Material Systems and MEMS: Design and Development Methodologies: Vijay K., 2017
3. The MEMS Handbook: Edited by Mohamed Gad-el-Hak, University of NotreDame, CRC Press LLC, 2015

COURSE OUTCOMES: After successful completion of the course, students will be able to:

1. Describethe basic concepts of MEMS, microfabrication, and smart materials.
2. Identifyand explainthe working principles of micro-sensors, actuators, and MEMS devices.
3. Demonstrate knowledge of various micro-fabrication processes used in MEMS manufacturing. 4. Analyse mechanical behaviour of MEMS structures using energy methods and elasticity concepts.
4. Apply FEM techniques for modelling and simulation of MEMS devices with piezoelectric elements.

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SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25237A2	**SYSTEM ON CHIP DESIGN (Programme Elective III)**	3	0	0	3	40	60	100

COURSE OBJECTIVES:

1. To introduce the fundamentals of SoC architecture, components, and design methodologies
2. To understand hardware-software co-design concepts including partitioning, scheduling, and hardware acceleration
3. To explore virtual prototyping, high-level synthesis, and system-level design methodologies
4. To examine SoC interconnection structures and protocols like AMBA AXI and Network-on-Chip (NoC).
5. To analyse performance and power at the system level using simulation platforms and case studies

UNIT-I: SoC Design Approach: Basics of Chips and SoC ICs, SoC Design: SoC CPU/IP Cores, Co-processor, Cache, DRAM Controller, SoC Synthesis, Static Timing Analysis (STA), Design for Testability, Verification, Physical Design.

UNIT-II: Processors Hardware-Software Co-Synthesis: Partitioning, Cycle Time, Die Area and Cost, Power, Area Time-Power Trade-offs and Chip Reliability, Real-Time Scheduling, Hardware Acceleration.

UNIT-III: Virtual Prototyping and High-Level Synthesis (HLS): Mapping High-Level Language Applications to Hardware, Transaction-Level Modeling and Electronic System Level Languages, Hardware Accelerators, Media Instructions, Coprocessors, System-Level Design Methodology, High-Level Synthesis (C-to-RTL), Hardware Synthesis and Architecture Techniques, Source-Level Optimizations.

UNIT-IV: SoC Interconnection Structures: Bus-Based Interconnection, Bus Protocols: AMBA AXI Bus, AXI4-Stream, IBM Core Connect, Avalon. Interconnection structures, Network on Chip (NoC) Interconnection and NoC Systems, IP Interfacing.

UNIT-V: Performance/Power Analysis of SoCs: System-Level Modeling and Integration, Simulation Platform for Performance Analysis of SoC/MPSoC, Use Cases and Examples.

TEXTBOOKS:

1. Veena Chakravarthi, A Practical Approach to VLSI System on Chip (SoC) Design – A Comprehensive Guide, Springer, 2020
2. S. Pasricha and N. Dutt, On-Chip Communication Architectures: System on Chip Interconnect, Morgan Kaufmann–Elsevier Publishers, 2008

REFERENCE BOOKS:

1. Keating, M., The Simple Art of SoC Design, Springer, 2011.
2. "Embedded System Design: A Unified Hardware/Software Approach"Authors: Frank Vahid and Tony Givargis, Publisher: Wiley

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Understand and estimate key design metrics and requirements including area, latency, Through put, energy, and power
2. Implement both hardware and software solutions, formulate hardware/software trade- offs, and perform hardware/software co-design
3. Analyse issues in system-on-chip design associated with interconnection structures, performance, and power consumption
4. Use System C programming and high-level synthesis (HLS) for design and modelling
5. Design and optimize a modern System-on-a-Chip

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25237B0	**DETECTION AND ESTIMATION THEORY (Programme Elective IV)**	3	0	0	3	40	60	100

COURSE OBJECTIVES: The course aims to:

1. To introduce fundamental concepts of random processes including Markov models, point processes, and Gaussian processes.
2. To develop understanding of detection theory using Bayesian and Neyman-Pearson approaches for signal classification under uncertainty.
3. To explore MMSE estimation techniques such as Wiener and Kalman filters for linear and nonlinear systems.
4. To provide knowledge of statistical inference including hypothesis testing, distribution estimation, and regression analysis.
5. To enable parameter estimation of random processes using model-free and model based approaches with spectral analysis tools.

UNIT –I

Random Processes: Discrete Linear Models, Markov Sequences and Processes, Point Processes, and Gaussian Processes.

UNIT –II

Detection Theory: Basic Detection Problem, Maximum A posteriori Decision Rule, Minimum Probability of Error Classifier, Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal a priori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT –III

Linear Minimum Mean-Square Error Filtering: Linear Minimum Mean Squared Error Estimators, Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT –IV

Statistics: Measurements, Nonparametric Estimators of Probability Distribution and Density Functions, Point Estimators of Parameters, Measures of the Quality of Estimators, Introduction to Interval Estimates, Distribution of Estimators, Tests of Hypotheses, Simple Linear Regression, Multiple Linear Regression.

UNIT –V

Estimating the Parameters of Random Processes from Data: Tests for Stationarity and Ergodicity, Model-free Estimation, Model-based Estimation of Autocorrelation Functions, Power Special Density Functions.

TEXT BOOKS:

1. Steven M. Kay, "Fundamentals of Statistical signal processing, volume-1: Estimation theory". Prentice Hall 2011
2. Steven M. Kay, "Fundamentals of Statistical signal processing, volume-2: Detection theory". Prentice Hall 2011.

REFERENCE BOOKS:

1. Harry L. Van Trees, "Detection, Estimation, and Modulation Theory, Part I," John Wiley & Sons, Inc. 2011.
2. A. Papoulis and S. Unnikrishna Pillai, "Probability, Random Variables and stochastic processes, 4e". The McGraw-Hill 2010

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Demonstrate understandingof random processes, including discrete linear models, Markov processes, point processes, and Gaussian processes relevant to signal processing.
2. Apply detection theory to solve problems using MAP, Bayes, and Neyman-Pearson decision rules for both binary and multiple hypothesis testing.
3. Develop and analyze linear and nonlinear minimum mean square error (MMSE) estimators, and design digital Wiener and Kalman filters for signal estimation.
4. Estimate and interpret statistical parameters and distributions using point estimation, nonparametric methods, interval estimates, hypothesis testing, and linear regression models.
5. Evaluate stationarity and ergodicity of random processes and perform both model-free and model-based estimation of autocorrelation and power spectral density functions from data.

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COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25237B1	**EMI/ EMC (Programme Elective IV)**	3	0	0	3	40	60	100

OBJECTIVES:

1. To introduce enough knowledge regarding theElectromagnetic interference/ Electromagnetic compatibility, Its practical experiences andconcerns, and various sources both the natural and nuclear sources of EMI.
2. To know the practical experiences due to EMI such as mainspower supply, switches and relaysetc and Analyse EM Propagation and Crosstalk
3. To know various methods of themeasurements radiated and conducted interference in open area test sites and in chambers.
4. To Learn about the various methods of minimizing the EMI.
5. To know the National/International EMC Standards.

UNIT -I: Introduction, Natural and Nuclear Sources of EMI / EMC:

Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations, An overview of EMI / EMC, Natural and Nuclear sources of EMI.

UNIT -II: EMI from Apparatus, Circuits and Open Area Test Sites:

Electromagnetic emissions, Noise from relays and switches, Non-linearities in circuits, passive intermodulation, Cross talk in transmission lines, Transients in power supply lines, Electromagnetic interference (EMI), Open area test sites and measurements.

UNIT -III: Radiated and Conducted Interference Measurements and ESD: Anechoic chamber, TEM cell, GH TEM Cell, Characterization of conduction currents / voltages, Conducted EM noise on power lines, Conducted EMI from equipment, Immunity to conducted EMI detectors and measurements, ESD, Electrical fast transients / bursts, Electrical surges.

UNIT -IV: Grounding, Shielding, Bonding and EMI filters:

Principles and types of grounding, Shielding and bonding, Characterization of filters, Power lines filter design.

UNIT -V: Cables, Connectors, Components and EMC Standards:

EMI suppression cables, EMC connectors, EMC gaskets, Isolation transformers, optoisolators, National / International EMC standards.

TEXTBOOKS:

1. Engineering Electromagnetic Compatibility - Dr. V.P. Kodali, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
2. Electromagnetic Interference and Compatibility IMPACT series, IIT – Delhi, Modules 1-9

REFERENCE BOOKS:

1. Introduction to Electromagnetic Compatibility - Ny, John Wiley, 1992, by C.R. Pal.
2. Noise Reduction Techniques in Electronic Systems" – Henry W. Ott

COURSE OUTCOMES: At the end of this course the student can be able to:

1. Understand the electromagnetic environment the definitions of EMI and EMC, history of EMI some examples of practical experiences due to EMI such as mains power supply, switches and relays etc.
2. Understand the celestial electromagnetic noise the occurrence of lightning discharge and their effects, the charge accumulation and discharge in an electrostatic discharge, model ESD wave form, the various cases of nuclear explosion and the transients.
3. Understand the methods to measure RE and RS in the open are test sites
4. Understand the measurement facilities and procedures using anechoic chamber, TEM cell, reverberating chamber GTEM cell.
5. Apply grounding, shielding, bonding techniques, and design EMI filters for interference mitigation.

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D25237B2	**ARM CONTROLLERS AND EMBEDDED C (Programme Elective IV)**	3	1	0	4	40	60	100

COURSE OBJECTIVES:

1. To introduce ARM processor architecture, instruction sets, and efficient programming techniques.
2. To explore exception handling, memory hierarchy, and management units in ARM systems.
3. To develop embedded system applications using ARM Cortex-M microcontrollers.
4. To implement peripheral interfacing techniques including UART, ADC/DAC, and GPIO.
5. To understand communication protocols like I²C and SPI through practical case studies.

UNIT- I:

ARM Processor Fundamentals: ARM Design Philosophy, Registers, CPSR, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions.
Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Load –Store Instructions, Software Interrupt Instruction, PSR Instructions.
Introduction to the Thumb Instruction Set: Thumb Register Usage, Branch Instructions, Data Processing Instructions, Load-Store Instructions, Stack instructions, Software Interrupt Instruction.
Efficient C Programming: Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Structure Arrangement.
Writing and Optimizing ARM Assembly Code: Writing Assembly Code, Profiling and Cycle Counting, Instruction Scheduling, Register Allocation, Conditional Execution, Looping Constructs.

UNIT- II:

Exception and Interrupt Handling: Exception Handling, Interrupts, Interrupt Handling Schemes
Caches: The Memory Hierarchy and Cache Memory, Cache Architecture, Cache Policy, Flushing and Cleaning Cache Memory.
Memory Protection Units: Protected Regions, Initializing the MPU, Caches and Write Buffer.
Memory Management Units: Moving from an MPU to an MMU, How Virtual Memory Works, Details of the ARM MMU, Page Tables, Translation Lookaside Buffer, Domains And Memory Access Permission, The Fast Context Switch Extension

UNIT- III:

Introduction: Definition of Embedded Systems, Real life examples of embedded systems, Basics of Developing for Embedded Systems
ARM Instruction set Architecture: ARM Cortex-M Organization, Arithmetic, Logical and Shift instructions, Data Movement Instructions, Branch instructions, Program Status register, Bitwise logic operations, Sign and Zero extension, Data Comparison, Memory addressing, Branch and conditional execution, Control structures, Subroutines, 64-bit data processing.
GPIO: GPIO Input Modes, GPIO Output Modes, Memory-mapped I/O, Push button, Programming exercises on GPIO and Push-button
General-purpose Timers: Clock Configuration, Timer Organization, and Counting Modes, Timer Update Events, PWM Registers, Configuration and initialization of PWM block, Programming exercises on the selection of clock source, Timer's concept, and PWM

UNIT- IV:

UART: UART Block, UART Registers, UART baud rate calculation, Configuration and initialization of UART
ADC/DAC: ADC & DAC registers, pin configuration, ADC modes, Configuring ADC and DAC module, Programming exercises on ADC and DAC
Interfacing: Keypad, LCD, and Seven segment display interfacing with ARM Cortex-M3 Microcontroller.

UNIT-V:

Inter-Integrated Circuit (1^2C): I^2C operating modes, Configuration of I^2C, Interface a sensor using I^2C protocol.
Serial Peripheral Interface (SPI): SPI Modes, Master operation, Slave operation, Configuration of SPI

Case Study: Smart Home-Smart Door Locks and Interface a temperature sensor with an I^2C Module to measure the room temperature.

TEXTBOOKS:

1. A.Sloss, D.Symes, C.Wright, "ARM system Developers Guide: Designing and Optimizing System Software", Morgan Kaufmann publishers, 2012.
2. Dr.Yifeng Zhu "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly and C" Third edition, 2018.

REFERENCE BOOKS:

1. Steve Furber, "ARM System on Chip Architecture", 2nd ed., Addison Wesley Professional,2000.
2. Valvano, J,"Embedded microcomputer systems: real time interfacing", 3rd Edition, Cengage Learning, 2011.
3. Frank Vahid, TonyGivargis, "Embedded System Design", J Wiley India,2005.
4. Ariel Lutenberg, Pablo Gomez, Eric Pernia "A Beginner's Guide to Designing Embedded System Applications on Arm Cortex-M Microcontrollers"
5. Qing Li, Caroline Yao "Real-time concepts for Embedded Systems" CMP books.

COURSE OUTCOMES: After completion of the course, students will be able to:

1. Demonstrate proficiency in ARM instruction sets and assembly code optimization.
2. Configure and manage exceptions, interrupts, and memory systems in ARM-based designs Develop embedded applications using GPIO, timers, and control structures.
3. Interface and program peripherals such as UART, ADC/DAC, and display modules.
4. Apply I^2C and SPI protocols in real-world scenarios like smart home systems

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2523790	**INTERNET OF THINGS LABORATORY**	0	1	2	2	40	60	100

COURSE OBJECTIVES:

1. To introduce students to the fundamentals of IoT architecture and physical layer components.
2. To familiarize students with sensors, actuators, transducers, microcontrollers, and microprocessors used in IoT.
3. To provide hands-on experience with Arduino, Scratch programming, S4A tool, and Arduino IDE.
4. To develop practical skills using Tinker cad simulations and real-time Arduino-based interfaces.
5. To enable interfacing of digital and analogy sensors and actuators with Arduino for real-time applications.

List of Experiments:

1. Introduction to IoT, IoT Architecture, introduction to Physical layer
2. Introduction to sensors, actuators, and transducers. Introduction to microcontrollers and microprocessors
3. Introduction to Arduino. Introduction to Scratch programming, S4A tool, and Arduino IDE.
4. Introduction to Tinker cad and some practical examples
5. Working with analog, digital inputs & outputs
6. Interfacing Arduino with Embedded sensors and Actuators
7. Interfacing Arduino with additional sensors
8. Working on Displays and interfacing with Arduino
9. Arduino & LCD Based Projects

10. Arduino interfacing with Keypad and its operation
11. Creating the app (app designing using MIT) and controlling your hardware with your app.
12. Introduction to NodeMCU and basic tasks
13. Introduction to Cloud, some IoT Cloud Platforms publishing sensor data to a cloud using Thing speak.
14. Controlling your sensor data using Thing speak and MIT APP Inventor
15. Email notifications, app alerts using Blynk cloud 16. Home Automation Using Blynk app

COURSE OUTCOMES: At the end of the Course the student shall be able to

1. Analyze the concepts of IoT along with its applications.
2. Design a prototype using Arduino Uno.
3. Analyze different types of sensors, actuators and communication Protocols.
4. Execute a prototype of Home Automation using Blynk app.
5. Design an IoT application to interact with cloud.

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COURSE STRUCTURE

M-Tech – I Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2523791	**EMBEDDED SYSTEM DESIGN LAB**	0	1	2	2	40	60	100

COURSE OBJECTIVES:

1. To introduce students to GPIO configuration and control in embedded systems.
2. To develop skills in serial communication between microcontrollers and PCs using UART.
3. To understand timer and counter functionalities for time delays and interrupts.
4. To provide experience with LCD interfacing and real-time message display.
5. To implement analogy-to-digital conversion and PWM signal generation for control applications.

Experiments using ARM Cortex-M Microcontroller

(NUCLEO board -F429ZI):

1. Program to configure and control General Purpose Input / Output (GPIO) port pins.
2. Program to demonstrate Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
3. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment.
4. Program to demonstrate a simple interrupt handler and setting up a timer.
5. Program to Displaying a message in a 2-line x 16 Characters LCD display and verify the result in debug terminal.
6. Program to demonstrate ADC interfacing.
7. Generation of PWM Signal with the objective of introducing the practical application of timers and fundamental principles of control theory.

8. To integrate a micro-SD card with the computing system for the purpose of storing event logs conveniently on the SD card.
9. To establish a connection between the two computing systems using Bluetooth Low Energy (BLE), with the objective of monitoring pertinent information from one system and facilitating gate control through the other system.
10. To enhance the smart home system by enabling it to host a web page through Wi-Fi connectivity, thereby allowing users to access information using a smartphone or PC.

COURSE OUTCOMES (POS):

After successful completion of this lab course, students will be able to:

1. Configure and control GPIO ports and interface with external devices.
2. Implement UART-based serial communication and use debug terminals for testing.
3. Apply timers and counters for generating delays and handling interrupts in real-time systems.
4. Interface LCDs, ADC modules, and generate PWM signals for embedded applications.
5. Store and retrieve event data using SD card integration.

Dr. Samuel George Institute of Engineering & Technology
(An Autonomous Institute with NAAC 'A' Grade)
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SGIT-R25 M.TECH (DIGITAL ELECTRONICS & COMMUNICATION ENGINEERING)

COURSE STRUCTURE

M-Tech – II Semester

Course Code	Course Name	Course Structure				Internal Marks	External Marks	Total Marks
		L	T	P	C			
D2523780	**SEMINAR-II**	0	0	2	1	100	-	100